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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,448	11/12/2003	David G. Farber	TI-34917.1	8697

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EXAMINER	
BEREZNY, NEMA O	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/712,448	FARBER ET AL.	
	Examiner	Art Unit	
	Nema O. Berezny	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *43-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *43-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Preliminary Amendment, filed 11-12-03, which has been entered and considered. Claims 43-76 are pending; cancellation of claims 1-42 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 43-44, and 48 are rejected under 35 U.S.C. 102(b) as being anticipated by McDaniel (6,258,709). McDaniel discloses an integrated circuit comprising: a semiconductor substrate (Figs.2-9 el.10); a front-end structure (col.5 lines 31-41) coupled to said semiconductor substrate; and a first layer of a back-end structure (Fig.9) coupled to said front-end structure, said first layer of a back end structure having first layer interconnects (el.16) and first layer dielectrics (el.20); wherein a height of said first layer dielectrics is less than a height of said first layer interconnects (Fig.10; col.6 lines 58-62) **[claim 43]**; and wherein said first layer dielectrics comprises low-k material (col.6 lines 52-56) **[claim 44]**; and wherein said height of said first layer dielectrics are 10-30% less than said height of said first layer interconnects (Fig.10) **[claim 48]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 45, 60-62, and 65-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over McDaniel as applied to claims 43-44 above, and further in view of Li et al. (2002/0177322). McDaniel discloses wherein a height of a layer of dielectrics is less than a height of a layer of interconnects (Fig.10; col.6 lines 58-62). However, McDaniel does not disclose an OSG low-k material, a second layer of a back-end structure, or an interface region adjacent to an inside region of a second layer dielectric. McDaniel would look to one such as Li for higher quality openings, a multi-level metal interconnect, and electrical isolation between metal layers, respectively because Li discloses a low-k material comprising OSG (p.4 para.47) **[claims 45, 61, 62]**; a second layer of a back-end structure coupled to said first layer of a back end structure, said second layer of a back-end structure having second layer interconnects and second layer dielectrics (p.4 para.47) **[claim 60]**; and wherein an interface region is adjacent to an inside region of said second layer dielectric (p.4 para.47) **[claim 67]**. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the OSG layer, second layer back-end structure, and interface region of Li with the integrated circuit of McDaniel in order to provide better vertical openings [Kim

et al. (2003/0211750) – p.4 para.64], an increased number of devices on a single chip (Li – p.1 para.3), and provide intermediate electrical isolation (p.4 para.47), respectively.

Based upon the rejection of claim 60 above, McDaniel also discloses wherein said height of said second layer dielectrics are 10-30% less than said height of said second layer interconnects (Fig.10) **[claim 65]**; and wherein at least one of said first layer interconnects is electrically connected to at least one of said second layer interconnects at an interface region (Fig.11) **[claim 66]**.

Claims 46, 49, 51-54, 56-59, 63, and 68-76 are rejected under 35 U.S.C. 103(a) as being unpatentable over McDaniel in view of Li as applied to claims 43 above, and further in view of Yu et al. (6,372,632). McDaniel in view of Li do not disclose copper interconnects or a barrier layer. However, McDaniel and Li would look to one such as Yu for speed enhancement and adherence to the low-k material because Yu discloses wherein said first layer interconnects comprise copper (Fig.6 el.14; col.4 lines 44-46); and a barrier layer (el.18) coupled to said first layer of a back-end structure. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the copper interconnects and barrier layer of Yu with the integrated circuit of McDaniel and Li. Copper interconnects provide higher conductivity for interconnect routing, operate with less power, and provide speed enhancement for very small features [Ho et al. (2002/0108929) – p.2 para.22] **[claims 46, 54, 63]**. A barrier layer prevents the copper interconnect from diffusing into the low-k material and permits the copper layer to adhere to the low-k material (Yu – col.4 lines 39-41) **[claims 49]**.

Based upon the rejection of claims 43 and 49 above, McDaniel in view of Li disclose a second layer of a back-end structure coupled to said first layer of a back end structure, said second layer of a back-end structure having second layer interconnects and second layer dielectrics (Li - p.4 para.47), wherein a height of a layer of dielectrics is less than a height of a layer of interconnects (McDaniel - Fig.10; col.6 lines 58-62) **[claim 51]**.

Based upon the rejection of claim 51 above, McDaniel discloses wherein said height of said second layer dielectrics are 10-30% less than said height of said second layer interconnects (Fig.10) **[claim 56]**; and wherein at least one of said first layer interconnects is electrically connected to at least one of said second layer interconnects at an interface region (Fig.11) **[claims 57, 68-76]**.

Based upon the rejection of claim 51 above, Li also discloses wherein said second layer dielectrics comprise low-k material (p.4 para.47) **[claim 52]**; wherein said low-k material comprises OSG (p.4 para.47) **[claim 53]**; and wherein said interface region is adjacent to an inside region of said second layer dielectric (p.4 para.47) **[claim 59]**.

Based upon the rejection of claim 57 above, Yu discloses wherein said interface region is adjacent to an inside region of said barrier layer (Fig.6 el.18) **[claim 58]**.

Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over McDaniel as applied to claim 43 above, and further in view of Takao (2003/0107069). McDaniel does not disclose both electrical signal and power interconnects. However,

McDaniel would look to one such as Takao for interconnection because Takao discloses wherein said first layer interconnects are metal lines that carry electrical signals and power (p.5 para.79,80). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the signal and power interconnects of Takao with the integrated circuit of McDaniel in order to connect intermediate conductive layers with wire layers of a memory cell (p.5 para.79).

Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over McDaniel in view of Li and Yu as applied to claims 43, 49, and 51 above, and further in view of Takao (2003/0107069). McDaniel, Li and Yu do not disclose both electrical signal and power interconnects. However, McDaniel, Li and Yu would look to one such as Takao for interconnection because Takao discloses wherein said first layer interconnects are metal lines that carry electrical signals and power (p.5 para.79,80). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the signal and power interconnects of Takao with the integrated circuit of McDaniel, Li and Yu in order to connect intermediate conductive layers with wire layers of a memory cell (Takao - p.5 para.79).

Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over McDaniel in view of Li as applied to claims 43 and 60 above, and further in view of Takao (2003/0107069). McDaniel and Li do not disclose both electrical signal and power interconnects. However, McDaniel and Li would look to one such as Takao for

interconnection because Takao discloses wherein said first layer interconnects are metal lines that carry electrical signals and power (p.5 para.79,80). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the signal and power interconnects of Takao with the integrated circuit of McDaniel and Li in order to connect intermediate conductive layers with wire layers of a memory cell (Takao - p.5 para.79).

Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over McDaniel in view of Yu as applied to claims 43 and 49 above, and further in view of Seo et al. (2003/0116439). McDaniel in view of Yu do not disclose a SiC barrier layer. However, McDaniel in view of Yu would look to one such as Seo for high thermal conductivity because Seo discloses wherein said barrier layer comprises SiC (p.5 para.42). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the SiC barrier layer of Seo with the integrated circuit of McDaniel and Yu. Silicon carbide has a wide bandgap, high thermal conductivity, high saturated electron drift velocity, and high electron mobility [Li (2002/0177322) – p.3 para.40].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O. Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB

Craig A. Thompson

CRAIG A. THOMPSON
PRIMARY EXAMINER